What Is Claimed Is:

1. A memory system comprising:

an actual memory array comprising a plurality of cells, each of said plurality of cells storing a corresponding one of a plurality of data values;

a decoder to retrieve a signal from said actual memory according to an address;

an actual sense amplifier to sense said signal as a bit;

a latch latching said bit at a time point specified by a latch enable signal;

a dummy memory array offering a load when accessed; and

a dummy sense amplifier implemented similar to said actual sense amplifier, said dummy sense amplifier sensing an another signal which is received when said dummy memory array is accessed, said dummy sense amplifier generating said latch enable signal according to a time of completion of sensing said another signal,

wherein a positive correlation exists between an amount of said load and a delay in generating said another signal, wherein said dummy memory array is designed to offer said load such that said latch enable signal is generated in an appropriate time window to cause said bit to be latched.

2. The memory system of claim 1, wherein said dummy memory array, said dummy sense amplifier, said actual memory array, and said actual sense amplifier are all implemented in a same die.

3. The memory system of claim 1, wherein said dummy memory comprises an array of transistors.

4. The memory system of claim 3, wherein said array comprises a column of transistors.

5. The memory system of claim 4, wherein each of said column of transistors is implemented similar to transistors forming said actual memory array, wherein said column of transistors contain less than or equal to a number of transistors as a number of rows in said actual memory array.

6. The memory system of claim 4, wherein each of said column of transistors is implemented to be of a higher drive strength than the drive strength of transistors forming said actual memory array.

7. The memory system of claim 4, wherein each of said transistor comprises a NMOS transistor having a gate to source voltage equaling zero, and wherein a drain terminal of said NMOS transistor is connected to a dummy bit line, said dummy bit line being connected to said dummy sense amplifier.

8. The memory system of claim 7, wherein each of said dummy sense amplifier and said actual sense amplifier comprises:

a first transistor having a drain terminal connected to a supply voltage and a gate terminal connected to a sense enable signal;

a second transistor and a third transistor, wherein said third transistor is implemented

as a mirror of said second transistor, a gate terminal of said second transistor being connected to a gate terminal of said third transistor at a first node, a drain terminal of both of said second transistor and said third transistor being connected to a source terminal of said first transistor, a source terminal of said second transistor also being connected to said first node;

a resistive load connected to a source terminal of said third transistor at a second node;

an inverter having an input path connected to said second node; and

a fourth transistor having a drain terminal connected to said first node and a gate terminal connected to said sense enable signal.

9. The memory system of claim 8, in said dummy sense amplifier, wherein an output of said inverter is used to generate said latch enable signal, a first end of said dummy bit line being connected to said first node and a second end of said dummy bit line connected to a drain terminal of each of said array of transistors.

10. The memory system of claim 8, in said actual sense amplifier, wherein an output of said inverter represents a value retrieved from said actual memory, a first end of an actual bit line connected to said first node and a second end of said actual bit line connected to output of said decoder.

11. The memory system of claim 8, each of said plurality of cells comprises a transistor, said transistor being programmed to store one logic level if said actual bit line is connected to a drain terminal of said transistor and another logic level otherwise.

12. The memory system of claim 1, wherein said actual memory array comprises a compiler memory.

13. The memory system of claim 1, wherein said dummy memory array and dummy sense amplifier are contained in a tracking circuit, and said tracking circuit is implemented without reference signals.

14. A tracking circuit to indicate an appropriate time point at which to sense a signal received from an actual memory array comprising a plurality of cells, each of said plurality of cells storing a corresponding one of a plurality of data values, said tracking circuit comprising:

an actual sense amplifier to sense said signal as a bit;

a dummy memory array offering a load when accessed; and

a dummy sense amplifier implemented similar to said actual sense amplifier, said dummy sense amplifier sensing an another signal which is received when said dummy memory array is accessed, said dummy sense amplifier generating said latch enable signal according to a time of completion of sensing said another signal,

wherein a positive correlation exists between an amount of said load and a delay in generating said another signal, wherein said dummy memory array is designed to offer said load such that said latch enable signal is generated in an appropriate time window to cause said bit to be latched.

15. The tracking circuit of claim 14, wherein said dummy memory comprises an

array of transistors.

16. The tracking circuit of claim 15, wherein said array comprises a column of transistors.

17. The tracking circuit of claim 16, wherein each of said column of transistors is implemented similar to transistors forming said actual memory array, wherein said column of transistors contain less than or equal to a number of transistors as a number of rows in said actual memory array.

18. The tracking circuit of claim 16, wherein each of said column of transistors is implemented to be of a higher drive strength than the drive strength of transistors forming said actual memory array.

19. The tracking circuit of claim 16, wherein each of said column of transistors comprises a NMOS transistor having a gate to source voltage equaling zero, and wherein a drain terminal of said NMOS transistor is connected to a dummy bit line, said dummy bit line being connected to said dummy sense amplifier.

20. The tracking circuit of claim 16, wherein each of said dummy sense amplifier and said actual sense amplifier comprises:

a first transistor having a drain terminal connected to a supply voltage and a gate terminal connected to a sense enable signal;

a second transistor and a third transistor, wherein said third transistor is implemented as a mirror of said second transistor, a gate terminal of said second transistor being connected to a gate terminal of said third transistor at a first node, a drain terminal of both of said second transistor and said third transistor being connected to a source terminal of said first transistor, a source terminal of said second transistor also being connected to said first node;

a resistive load connected to a source terminal of said third transistor at a second node;

an inverter having an input path connected to said second node; and

a fourth transistor having a drain terminal connected to said first node and a gate terminal connected to said sense enable signal.

21. The tracking circuit of claim 20, in said dummy sense amplifier, wherein an output of said inverter is used to generate said latch enable signal, a first end of said dummy bit line being connected to said first node and a second end of said dummy bit line connected to a drain terminal of each of said array of transistors.